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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,316	02/08/2002	Junichi Karasawa	81751.0029	9698

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EXAMINER	
LOKE, STEVEN HO YIN	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 02/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/072,316	KARASAWA ET AL.
	Examiner	Art Unit
	Steven Loke	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 13-18* is/are rejected.

7)☒ Claim(s) *11 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

3. The disclosure is objected to because of the following informalities:

In page 16, line 23, it is believed that the first gate-gate electrode layer 20 pass between layer 16b and layer 16c instead of layer 16a and layer 16c.

In page 16, line 26, it is believed that layer 16b, layer 16c and electrode layer 20 instead of layer 16a, layer 16c and electrode layer 20 form transistor Q3.

Appropriate correction is required.

4. Claims 13 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 13, it is unclear how the first gate-gate electrode layer, the second gate-gate electrode layer and the first drain-gate wiring layer are located in a single first conductive layer. It is believed that the first gate-gate electrode layer, the second gate-gate electrode layer and the first drain-gate wiring layer are located in a first conductive layer level of the SRAM.

In claim 13, it is also unclear how the first drain-drain wiring layer, the second drain-drain wiring layer and the lower layer are located in a single second conductive layer. It

is believed that the first drain-drain wiring layer, the second drain-drain wiring layer and the lower layer are located in a second conductive layer level.

In claim 14, line 2, the phrase "the second conductive layer" has no antecedent basis. Claim 1 never discloses a second conductive layer in a memory cell.

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-10 and 16 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Natsume.

In regards to claim 1, Natsume shows all the elements of the claimed invention in figs. 1-21. It is a semiconductor device provided with a memory cell including a first driver transistor D2, a second driver transistor D1, a first transfer transistor T2, a second transfer transistor T1, a first load transistor P2 and a second load transistor P1. The semiconductor transistor comprising: a first gate-gate electrode layer [10] including a gate electrode of the first load transistor P2 and a gate electrode of the first driver transistor D2; a second gate-gate electrode layer [9] including a gate electrode of the second load transistor P1 and a gate electrode of the second driver transistor D1; a first drain-drain wiring layer [27] which forms a part of a connection layer that electrically connects a drain region of the first load transistor P2 and a drain region of the first driver

transistor D2; a second drain-drain wiring layer [16] which forms a part of a connection layer that electrically connects a drain region of the second load transistor P1 and a drain region of the second driver transistor D1; a first drain-gate wiring layer [10] which forms a part of a connection layer that electrically connects the first gate-gate electrode layer [10] and the second drain-drain wiring layer [16]; a second drain-gate wiring layer [27] which forms a part of a connection layer that electrically connects the second gate-gate electrode layer [9] and the first drain-drain wiring layer [27]; and a first active region in which the first load transistor P2 is provided, wherein the first drain-gate wiring layer [10] and the second drain-gate wiring layer [27] are located in different layers, respectively, and wherein a first protruded active region is provided in a manner to protrude from an end portion of the first active region.

In regards to claim 2, Natsume further discloses the first protruded active region is provided in a manner to protrude on a side opposite to a side where the first and second driver transistors [D2, D1] are provided.

In regards to claim 3, Natsume further discloses a part of the first active region and the first protruded active region form an L-shape.

In regards to claim 4, Natsume further discloses a second active region in which the second load transistor P1 is provided; and a second protruded active region provided in a manner to protrude from an end portion of the second active region.

In regards to claim 5, Natsume further discloses the second protruded active region is provided in a manner to protrude on a side opposite to a side where the first and second driver transistors [D2, D1] are provided.

In regards to claim 6, Natsume further discloses a part of the second active region and the second protruded active region form an L-shape.

In regards to claim 7, Natsume further discloses the first drain-gate wiring layer [10] is electrically connected to the second drain-drain wiring layer [16] through a contact section (fig. 14(b)), and wherein the second drain-gate wiring layer [27] is electrically connected to the second gate-gate electrode layer [9] through a contact section [18], and electrically connected to the first drain-drain wiring layer [27] through a contact section.

In regards to claim 8, Natsume further discloses the first drain-gate wiring layer [10] is located in a layer lower than the second drain-gate wiring layer [27].

In regards to claim 9, Natsume further discloses the first drain-gate wiring layer [10] is located in a layer in which the first gate-gate electrode layer [10] is provided.

In regards to claim 10, Natsume further discloses the second drain-gate wiring layer [27] is formed across a plurality of layers [10, 16, 9].

In regards to claim 16, Natsume shows all the elements of the claimed invention in figs. 1-21. It is a semiconductor device using as a memory cell a flip-flop including a first load transistor P2, a first driver transistor D2, a second load transistor P1 and a second driver transistor D1, wherein the first and second load transistors in one memory cell are disposed symmetrically about a straight line extending in a gate width direction between the drain regions of the first and second load transistors, and wherein each of the drain regions of the first and second load transistors includes a protruded active region protruding in the gate width direction beyond an end of a channel region.

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Natsume.

In regards to claim 15, Natsume differs from the claimed invention by not showing the second conductive layer has a thickness of 100 nm to 200 nm. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the second conductive layer has a thickness of 100 nm to 200 nm, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

9. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Natsume as applied to claims 1-10, 15 and 16 above, and further in view of Song.

In regards to claim 17, Natsume differs from the claim invention by not showing the memory cell of claims 1-10, 15 and 16 can be applied to a memory system.

Song shows SRAMs are widely used for cache memory devices (col. 1, lines 15-16).

Since both Natsume and Song teach a SRAM for semiconductor memory, it would have been obvious to have the memory cell of Natsume in the cache memory devices of Song because it improves the α-ray soft error resistance of the SRAM.

In regards to claim 18, Natsume differs from the claim invention by not showing the memory cell of claims 1-10, 15 and 16 can be applied to an electronic apparatus.

Song shows SRAMs are widely used for cache memory devices for computers (col. 1, lines 15-16).

Since both Natsume and Song teach a SRAM for semiconductor memory, it would have been obvious to have the memory cell of Natsume in the computers of Song because it improves the α-ray soft error resistance of the SRAM in the computers.

10. Applicant cannot rely upon the foreign priority papers to overcome the above rejections because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. Claims 16-18 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Madan.

In regards to claim 16, Madan shows all the elements of the claimed invention in figs. 5a and 6. It is a semiconductor device using as a memory cell a flip-flop including a first load transistor (PMOS in Quadrant 1), a first driver transistor (NMOS in Quadrant 3), a second load transistor (PMOS in Quadrant 2) and a second driver transistor

(NMOS in Quadrant 4), wherein the first and second load transistors in one memory cell are disposed symmetrically about a straight line extending in a gate width direction between the drain regions [608] of the first and second load transistors, and wherein each of the drain regions of the first and second load transistors includes a protruded active region protruding in the gate width direction beyond an end of a channel region.

In regards to claim 17, Madan further discloses a memory system (fig. 5a) provided with the semiconductor device of claim 16.

In regards to claim 18, Madan further discloses an electronic apparatus (col. 6, lines 29-32) provided with the semiconductor device of claim 16.

13. Claims 11 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is a statement of reasons for the indication of allowable subject matter: The major difference in the claim not found in the prior art of record is the second drain-gate wiring layer includes a lower layer of the second drain-gate wiring and an upper layer of the second drain-gate wiring layer, and wherein the upper layer is located in a layer over the lower layer, and electrically connected to the lower layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers

for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

sl
February 9, 2003

Steven Loke